REMARKS

Claims 1-49 are pending in the present application. In the Office Action, claims 1, 3-4, 7, 10-17, 19-20, 22-23, 26, 29-32, 38-39, 41-43, 46, and 49 were rejected under 35 U.S.C. § 102(b) as allegedly being anticipated by Hohensee, et al (U.S. Patent No. 5,756,206). Claims 2, 18, 34-35, and 45 were rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Hohensee in view of Admitted Prior Art. Claims 5-6, 8, 24-25, 27, 36-37, 40, and 47-48 were rejected under 35 U.S.C. § 103(a) as allegedly being anticipated by Hohensee in view of Blonder (U.S. Patent No. 5,802,275). Claims 9, 21, 28, 33, and 44 were rejected under 35 U.S.C. § 103(a) as allegedly being anticipated by Hohensee in view of Slassi (U.S. Patent No. 6,435,416). The Examiner's rejections are respectfully traversed.

With regard to independent claims 1, 11-13, and 30, Applicants describe and claim a security check unit coupled to receive a physical address within a selected memory page and security attributes of the selected memory page. The claimed security check unit is configured to use the physical address to access at least one security attribute data structure located in the memory to obtain an additional security attribute of the selected memory page, and to generate a fault signal dependent upon the security attributes of selected memory page and the additional security attribute of the selected memory page. Independent claim 41 describes and claims a method that may be used by the security check unit.

Hohensee describes a memory management unit 14 that may, among other things, transform a virtual address to a physical address used to access memory. The virtual address space is associated with a plurality of segments, each of which is associated with a segment register 30(0-M). Each segment register 30(m) contains a pointer that identifies one of a plurality of segment descriptors 31(0-M) in a segment descriptor table 31. Each segment descriptor 31(0-

M) generally includes three fields, including an access rights field 32(0-M), a segment length field 33(0-M), and a segment base address field 34(0-M). If an access operation is not within the access rights indicated by the access rights field 32(0-M), the access operation will not proceed. If the access operation is within the access rights indicated by the access rights field 32(0-M) associated with the segmented virtual address, the access operation may proceed and the segmented virtual address may be coupled to a virtual address translator 44, which translates the segmented virtual address to a physical address in a conventional manner. See Hohensee, col. 7-8 and Figure 2.

However, Applicants respectfully submit that Hohensee does not use the physical address to access at least one security attribute data structure located in the memory to obtain an additional security attribute of the selected memory page. As discussed above, Hohensee uses the access rights indicated by the access rights field 32(0-M) associated with the segmented virtual address to determine if an access operation is permitted. Accordingly, Hohensee does not generate a fault signal dependent upon the security attributes of selected memory page and the additional security attribute of the selected memory page that is accessed using the physical address. Thus, Applicants respectfully submit that claims 1, 3-4, 7, 10-17, 19-20, 22-23, 26, 29-32, 38-39, 41-43, 46, and 49 are not anticipated by Hohensee and request that the Examiner's rejections of these claims under 35 U.S.C. 102(b) be withdrawn.

Moreover, it is respectfully submitted that the pending claims are not obvious in view of the cited references, either alone or in combination. To establish a *prima facie* case of obviousness, three basic criteria must be met. First, the prior art reference (or references when combined) must teach or suggest all the claim limitations. *In re Royka*, 490 F.2d 981, 180 U.S.P.Q. 580 (CCPA 1974). Second, there must be some suggestion or motivation, either in the

references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. That is, there must be something in the prior art as a whole to suggest the desirability, and thus the obviousness, of making the combination. *Panduit Corp. v. Dennison Mfg. Co.*, 810 F.2d 1561 (Fed. Cir. 1986). In fact, the absence of a suggestion to combine is dispositive in an obviousness determination. *Gambro Lundia AB v. Baxter Healthcare Corp.*, 110 F.3d 1573 (Fed. Cir. 1997). The mere fact that the prior art can be combined or modified does not make the resultant combination obvious unless the prior art also suggests the desirability of the combination. *In re Mills*, 916 F.2d 680, 16 U.S.P.Q.2d 1430 (Fed. Cir. 1990); M.P.E.P. § 2143.01. Third, there must be a reasonable expectation of success. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 U.S.P.Q.2d 1438 (Fed. Cir. 1991); M.P.E.P. § 2142. A recent Federal Circuit case emphasizes that, in an obviousness situation, the prior art must disclose each and every element of the claimed invention, and that any motivation to combine or modify the prior art must be based upon a suggestion in the prior art. *In re Lee*, 61 U.S.P.Q.2d 143 (Fed. Cir. 2002). Conclusory statements regarding common knowledge and common sense are insufficient to support a finding of obviousness. *Id.* at 1434-35.

As discussed above, Hohensee does not describe using a physical address to access at least one security attribute data structure located in a memory to obtain an additional security attribute of a selected memory page or generating a fault signal dependent upon the security attributes of selected memory page and the additional security attribute of the selected memory page. Moreover, Hohensee is concerned with emulating a segmented virtual address space using a microprocessor that provides a non-segmented virtual address space and therefore provides no

suggestion or motivation for using a physical address to access the at least one security attribute data structure located in the memory to obtain an additional security attribute of the selected memory page or generating a fault signal dependent upon the security attributes of selected memory page and the additional security attribute of the selected memory page.

The Examiner relies upon the Admitted Prior Art to teach a user/supervisor bit and a read/write bit as defined by the x86 processor architecture, Blonder to teach a Secure Page bit, and Slassi to teach a secure execution mode bit. However, neither the cited references nor the Admitted Prior Art remedy the aforementioned fundamental deficiencies of the primary reference. Thus, Applicants respectfully submit that claims 2, 5-6, 8-9, 18, 21, 24-25, 27-28, 33-37, 40, 44-45, and 47-48 are not obvious over the cited references for at least the aforementioned reasons and request that the Examiner's rejections of these claims under 35 U.S.C. 103(a) be withdrawn.

For the aforementioned reasons, it is respectfully submitted that all claims pending in the present application are in condition for allowance. The Examiner is invited to contact the undersigned at (713) 934-4052 with any questions, comments or suggestions relating to the referenced patent application.

Respectfully submitted,

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